

Course Description

As FPGA designs become increasingly more complex, designers are searching to reduce design and debug time. The powerful, yet easy-to-use ChipScope™ Pro tool solution helps minimize the amount of time required for debug and verification. This one-day course will show you effective ways to debug logic and high-speed designs—thereby decreasing your overall design development time. This training will provide hands-on labs that demonstrate how the ChipScope Pro tools can address advanced verification and debugging challenges.

Level – Intermediate

Course Duration – 1 day

Price – \$700 or 7 Training Credits

Course Part Number – CSP22000-92-ILT

Who Should Attend? – Logic, high-speed and embedded designers looking to minimize debug and verification time

Prerequisites

- FPGA design experience or completion of the Xilinx *Fundamentals of FPGA Design* course
- ChipScope Pro Software REL strongly recommended (www.xilinx.com/support/training/rel/chipscopepro-rel.htm)

Software Tools

- ISE™ 9.2i software
- ChipScope Pro 9.2i software
- ChipScope Pro Serial I/O Toolkit 9.2i*
- Agilent Logic Analyzer Application Software*

After completing this comprehensive training, you will have the necessary skills to:

- Maximize ChipScope Pro tool core performance
- Minimize negative timing impacts on a design
- Use techniques that enhance and extend the capabilities of the ChipScope Pro tools
- Enable and identify the advantages of remote debugging
- Analyze, set up, and debug high-speed serial I/O designs*
- Use the Agilent solutions to overcome storage issues and perform a system-level debug*

Course Outline

- Agenda and Introduction
- **Lab:** Adding the ILA Core to an Existing Design and/or Adding the ILA and VIO Cores for Remote Monitoring and Control
- Timing Implications
- **Demo:** Minimizing ILA Core Impact with the PlanAhead Software
- Tips and Tricks
- **Lab:** Tips and Tricks
- Remote Debug
- **Lab:** Enabling Remote Debug*
- High-Speed Serial I/O Debug and Verification (Optional*)
- **Lab:** High-Speed Serial I/O Debug and Verification (Optional*)
- Agilent Solutions for Storage Qualification and System-Level Debug (Optional*)
- **Lab:** Inserting the Agilent ATC2 Measurement Core and Viewing Internal Activity with the FPGA Dynamic Probe (Optional*)
- **Lab:** Performing System-Level Debug with the Agilent FPGA Dynamic Probe (Optional*)

* Please check with Hardent to confirm whether this content is included with your specific class.

Lab Descriptions

- **Adding the ILA Core to an Existing Design** – You will use the Core Inserter tool flow for adding the ChipScope Pro tool ILA cores into a design to rapidly locate and solve a simple logic problem.
- **Adding the ILA and VIO Cores for Remote Monitoring and Control** – You will instantiate ICON, ILA, and VIO cores into a VHDL or Verilog design and practice monitoring signals of interest and externally driving select control signals.
- **Tips and Tricks** – This lab demonstrates the flexibility of the ChipScope Pro tool solution as you explore data qualification, cross-clock domain analysis, and oversampling techniques.
- **Enabling Remote Debug*** – This lab demonstrates how the ChipScope Pro tools can be used across a network. You will connect to another team's board, download your bitstream, and remotely monitor the other team's board on your machine.
- **High-Speed Serial I/O Debug and Verification*** – You will use the Xilinx ChipScope Pro Serial I/O Toolkit for the RocketIO™ transceivers in the Virtex™-5 FPGA. You will generate the ChipScope Pro tool IBERT design for the Virtex-5 XC5VLX50T device and customize it for the ML505 board. You will then connect two GTPs on the ML505 board and use the ChipScope Pro Analyzer tool to control the GTP parameters and monitor the effects.
- **Inserting the Agilent ATC2 Measurement Core and Viewing Internal Activity with the FPGA Dynamic Probe*** – You will leverage external memory resources by using the Agilent ATC2 Core, FPGA Dynamic Probe, and Virtual Logic Analyzer to address storage demands.
- **Performing System-Level Debug with the Agilent FPGA Dynamic Probe*** – You will see how the Agilent solution is used to reduce the time required to validate and determine the root cause of problems in FPGA-based systems.

Register Today

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