

Course Description

This course allows you to explore the System Generator tool and to gain the expertise you need to develop advanced, low-cost DSP designs. This intermediate course in implementing DSP functions focuses on learning how to use System Generator for DSP, design implementation tools, and hardware co-simulation verification. Through hands-on exercises, you will implement a design from algorithm concept to hardware verification using the Xilinx FPGA capabilities.

Level – DSP 3

Course Duration – 2 days

Price – 1400\$ or 14 Training Credits

Course Part Number – DSP11000-11-ILT

Who Should Attend? – System engineers, system designers, logic designers, and experienced hardware engineers who are implementing DSP algorithms using the MathWorks MATLAB® and Simulink® software and want to use Xilinx System Generator for DSP design

Prerequisites

- Experience with the MATLAB and Simulink software
- Basic understanding of sampling theory

Software Tools

- Xilinx ISE® Design Suite: System Edition 11.1
- MATLAB with Simulink software R2008a or R2008b

After completing this comprehensive training, you will have the necessary skills to:

- Describe the System Generator design flow for implementing DSP functions
- Identify Xilinx FPGA capabilities and how to implement a design from algorithm concept to hardware simulation
- List various low-level and high-level functional blocks available in System Generator
- Identify the high-level blocks available for FIR and FFT designs
- Design a multiple-clock-based System Generator system
- Embed two System Generator designs into a larger design

Course Outline

Day 1

- Introduction to System Generator
- Simulink Software Basics
- **Lab 1:** Using the Simulink Software
- Basic Xilinx Design Capture
- **Lab 2:** Getting Started with Xilinx System Generator
- Signal Routing
- **Lab 3:** Signal Routing
- Implementing System Control
- **Lab 4:** Implementing System Control

Day 2

- Multi-Rate Systems
- **Lab 5:** Designing a MAC-Based FIR
- Filter Design
- **Lab 6:** Designing a FIR Filter Using the FIR Compiler Block
- Xilinx System Generator, Project Navigator, and Platform Studio Integration
- **Lab 7:** System Generator and Project Navigator Integration
- **Lab 8:** System Generator, Project Navigator, and Platform Studio Integration

Lab Descriptions

- **Lab 1:** Using the Simulink Software – Learn how to use the toolbox blocks in the Simulink software and design a system. Understand the effect sampling rate.
- **Lab 2:** Getting Started with Xilinx System Generator – Illustrates a DSP48-based (ML505 board) design. Perform hardware co-simulation verification targeting an ML505 board.
- **Lab 3:** Signal Routing – Design padding and unpadding logic by using signal routing blocks.
- **Lab 4:** Implementing System Control – Design an address generator circuit by using blocks and Mcode.
- **Lab 5:** Designing a MAC-Based FIR – Using a bottom-up approach, design a MAC-based bandpass FIR filter and verify through hardware co-simulation by using an ML505 board.
- **Lab 6:** Designing a FIR Filter Using the FIR Compiler Block – Design a bandpass FIR filter by using the FIR Compiler block to demonstrate increased productivity. Verify the design through hardware co-simulation by using the ML505 board.
- **Lab 7:** System Generator and Project Navigator Integration – Learn how to embed two System Generator designs into a larger design and how VHDL created by System Generator can be incorporated into the simulation model of the overall system.
- **Lab 8:** System Generator, Project Navigator, and Platform Studio Integration – Learn how to embed two System Generator designs into a larger design and how VHDL created by System Generator can be incorporated into the simulation model of the overall system.

Register Today

Hardent, the Authorized Training Provider (ATP) for Canada (excluding British Columbia), New England (Connecticut, Maine, Massachusetts, New Hampshire, Rhode Island and Vermont) and the Southeastern United States (Alabama, Florida, Georgia, Mississippi, North Carolina, South Carolina and Tennessee) delivers Xilinx public and private courses in your region. Visit www.hardent.com/training or contact Hardent's Training Coordinator for more information, to register for a class or to schedule a private course.

Email: training@hardent.com
Telephone: 514-999-3880



Turnkey Electronic Design

