

Course Description

This course shows you how to take advantage of the features available in the Xilinx FPGA architecture, including the Virtex™-4 FPGA, and describes how DSP algorithms can be implemented efficiently. The techniques also demonstrate which decisions at the system level have the greatest impact on the implementation process and product costs.

Level – Advanced

Course Duration – 3 days

Price – \$2100 or 21 Training Credits

Course Part Number – DSP20000-7-ILT

Who Should Attend? – Engineers and designers who have an interest in developing products that use digital signal processing

Prerequisites

A fundamental understanding of digital signal processing theory, including an understanding of the following principles:

- Sample rates
- Finite Impulse Response (FIR) and Infinite Impulse Response (IIR) filters
- Oscillators and mixers
- Fast Fourier Transform (FFT) algorithm

After completing this comprehensive training, you will have the necessary skills to:

- Describe how DSP algorithms can be implemented efficiently by using Xilinx FPGA technology
- Identify the capabilities and features of the various Xilinx FPGA families to implement efficient DSP algorithms
- Establish methods for the accurate estimation of silicon area consumption and cost
- Evaluate which algorithms are best suited for FPGA implementation and identify which algorithms are less desirable
- Assess how system-level decisions impact hardware implementation and how hardware implementation can enhance results at the system level

Course Outline

Day 1

- On the Same Wavelength
 - Basic terminology and acronyms used in DSP design
 - Sample rates and bit widths used in DSP applications
 - DSP building blocks and processing requirements
- Some Bits About Numbers
 - Numbering formats, range, and precision
 - Mathematical operations using a variety of formats
- Tuning the Receiver
 - Structure and Resources of Xilinx Devices
 - Estimating DSP building block sizes

Day 2

- Tuning the Receiver (continued)
 - Implementing the multiplication function
 - Bit-width impact on system-level decisions
- Memories are Made of This
 - Block versus distributed memory
 - SRL16E and the delay function
 - Memory aspect ratios and their manipulation
- Selective Filters
 - FIR filter specifications and implementation
 - Selecting a technique for a given specification
 - Effects of halfband and interpolated filters

Day 3

- One Filter Does Not Make a System
 - Options to be considered with multiple channels
 - Interpolation and decimation
 - Rate changing and its effect on FIR filter choice
 - Filtering algorithms that exploit device architecture
 - Importance of connectivity versus isolated functions
- Do Not Block the Datapath
 - Numeric controlled oscillators and mixers
 - Strategies for FFT implementation
 - Achieving bandwidth requirements of the FFT
 - Using the FPGA as an efficient co-processor

Course Exercises

- MAC Rates and Memory Requirements
- Constructing a 128-Tap FIR Filter
- Fractional Number Formats
- Twos Complement Arithmetic
- Summation by Addition Tree
- Summation by Addition Chain
- Full Adder: How Many Slices?
- Summation Structure Sizes
- Serial Summation Structure
- 8-Bit by 12-Bit Multiplier
- KCM Multipliers
- Distributed RAM for FIFO
- Size Estimates for Delay Structures
- Using the SRL16E as a FIFO
- Creating Larger RAM Structures
- Selecting a MAC FIR Technique
- Parallel FIR Filter Size
- Symmetry, Interpolation, and Phases
- Decimation Filter
- “fs/4” Mixing and Decimation
- Designing a Numeric Controlled Oscillator (NCO)
- FFT: Benchmarks and Transform Time
- Collection Time = Processing Time
- 128-Point FFT in 1.28 μ s

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