

Course Description

Become acquainted with the various solutions that Xilinx offers for Ethernet connectivity. Learn the basics of the Ethernet standard, protocol, and OSI model while applying Xilinx solutions via hands-on laboratory exercises. Perform simulation to understand fundamental principles and obtain the knowledge to assess hardware design considerations and software development requirements.

Level – Intermediate

Course Duration – 2 days

Price – \$1600 or 16 Training Credits

Course Part Number – EMAC23000-82-ILT

Who Should Attend? – Engineers who would like to come up to speed on utilizing Xilinx Ethernet connectivity solutions (soft cores and hard IP)

Prerequisites

- *Fundamentals of FPGA Design* course
- C programming knowledge recommended
- Experience with Xilinx ISE™ and Embedded Development Kit (EDK) software tools

Software Tools

- Xilinx ISE 8.2i
- Mentor Graphics ModelSim PE 6.0
- EDK 8.2

After completing this comprehensive training, you will have the necessary skills to:

- Identify Ethernet basics
- Utilize various Ethernet cores, used either in standalone mode or as a peripheral in a processor-based design
- Determine the appropriate core to use
- Develop software to drive the core and achieve desired functionality
- Integrate hard and soft IP into the Embedded Development Kit (EDK)

Course Outline

Day 1

- Ethernet Basics
- Network Protocols, Ethernet Interfaces, and Hardware
- **Lab 1:** Analyzing Ethernet Frames
- Physical Layer
- LocalLink Interface
- **Lab 2:** VLAN and Jumbo Frames
- Xilinx EMAC Solutions

Day 2

- **Lab 3:** Implementation
- EMAC and EMAC Lite
- **Lab 4:** EMAC Peripheral in Loopback Mode
- GEMAC
- TEMAC
- **Lab 5:** TEMAC in Loopback Mode
- 10GE MAC
- **Lab 6:** Analyzing 10GE MAC Frames

Lab Descriptions

- **Lab 1:** Analyzing Ethernet Frames – Understand components of Ethernet frames and how the packets flow. Analyze various packets and observe how the core reacts to MAC address changes.
- **Lab 2:** VLAN and Jumbo Frames – Modify the configuration register to enable and observe the effects of VLAN and jumbo frames. Understand statistics vectors.
- **Lab 3:** Implementation – Use CORE Generator™ software to generate a gigabit Ethernet core and then proceed with the implementation flow.
- **Lab 4:** EMAC Peripheral in Loopback Mode – Use the EDK to instantiate and connect the OPB EMAC peripheral to the OPB bus. Develop software to place the core in loopback mode.
- **Lab 5:** TEMAC in Loopback Mode – Use the EDK to instantiate a hard TEMAC and soft PLB TEMAC wrapper. Configure cores in scatter gather DMA mode. Use three programs to test the hardware in polled, simple DMA, and scatter/gather DMA modes after placing the hardware in loopback mode.
- **Lab 6:** Analyzing 10GE MAC Frames – Use the ModelSim simulator to perform functional simulation. Analyze various frames from XGMII and the client interface point of view.

Register Today

Hardent, the Authorized Training Provider (ATP) for Canada (excluding British Columbia), New England (Connecticut, Maine, Massachusetts, New Hampshire, Rhode Island and Vermont) and the Southeastern United States (Alabama, Florida, Georgia, Mississippi, North Carolina, South Carolina and Tennessee) delivers Xilinx public and private courses in your region. Visit www.hardent.com/training or contact Hardent's Training Coordinator for more information, to register for a class or to schedule a private course.

Email: training@hardent.com

Telephone: 514-999-3880

