

Course Description

Advanced FPGA Implementation tackles the most sophisticated aspects of the ISE® 10.1 design suite and Xilinx hardware. Seven labs provide hands-on experience in this two-day course and cover the Xilinx Synthesis Technology (XST) tools. This course requires the *Fundamentals of FPGA Design* and *Designing for Performance* courses as prerequisites. An intermediate knowledge of Verilog or VHDL is strongly recommended as is at least six months of design experience with Xilinx tools and FPGAs. The lecture material in this course covers the ISE 10.1 tools and the Virtex®-5 and Spartan®-3E FPGAs.

Level – Advanced

Course Duration – 2 days

Price – 1400\$ or 14 Training Credits

Course Part Number – FPGA33000-10-ILT

Who Should Attend? – Engineers who seek advanced training in using Xilinx tools to improve FPGA performance and utilization while also increasing productivity

Prerequisites

- *Fundamentals of FPGA Design*
- *Designing for Performance*
- Intermediate knowledge of Verilog or VHDL is strongly recommended
- At least six months' design experience with Xilinx tools and FPGAs

Software Tools

- Xilinx ISE Foundation™ 10.1 software with the ISE Simulator
- ChipScope™ Pro software
- Synplicity Synplify Pro 9.2 software

After completing this comprehensive training, you will have the necessary skills to:

- Implement designs via the Tcl command line
- Create and edit timing constraints in the UCF file
- Identify the I/O timing constraints and design modifications required for source-synchronous and system-synchronous interfaces
- Preserve design results by using SmartGuide™ technology or partitions
- Use the Floorplan Editor or Pinout and Area Constraints Editor (PACE) to create area constraints
- Change signals of interest in the ChipScope™ Pro tool for board-level debugging using the FPGA Editor

Course Outline

- Introduction
- **Lab 1:** Achieving Timing Closure and Review of Global Timing Constraints
- Tcl Scripting
- **Lab 2:** Tcl Scripting
- UCF Editing
- **Lab 3:** UCF Editing
- Advanced I/O Timing
- **Lab 4:** Advanced I/O Timing
- SmartCompile™ Technology Design Preservation Techniques
- **Lab 5:** SmartCompile Technology
- Floorplanning an Effective Layout
- **Lab 6:** Floorplanning

- FPGA Editor: Viewing and Editing a Routed Design
- **Lab 7:** Advanced FPGA Editor

Lab Descriptions

Note: Labs will be based on Xilinx ISE 10.1 software.

- **Lab 1:** Achieving Timing Closure and Review of Global Timing Constraints – Use the Constraints Editor to enter global timing constraints.
- **Lab 2:** Tcl Scripting – Write ISE tool control commands in a Tcl script file to implement the design. Then modify program switches to obtain the greatest possible performance from the design.
- **Lab 3:** UCF – Write constraints directly into a UCF file to guide the performance results of implementation.
- **Lab 4:** Advanced I/O Timing – Compose timing constraints for an I/O interface. Analyze the timing failures and determine changes to correct the timing issues. Modify the design to fix timing failures.
- **Lab 5:** SmartCompile Technology – Utilize SmartGuide technology and partitions to preserve the timing results from one iteration to the next.
- **Lab 6:** Floorplanning – Implement a design by using floorplanned constraints to enhance the timing results over a design without floorplanning.
- **Lab 7:** Advanced FPGA Editor – Use the FPGA Editor to view and edit a design. Rapidly locate and swap signals of interest for ChipScope Pro tool cores.

Register Today

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