

Course Description

This comprehensive course is a thorough introduction to the VHDL language. The emphasis is on writing Register Transfer Level (RTL) and behavioral source code. This class addresses targeting Xilinx devices specifically and FPGA devices in general. The information gained can be applied to any digital design by using a top-down synthesis design approach. This course combines insightful lectures with practical lab exercises to reinforce key concepts. You will also learn advanced coding techniques that will increase your overall VHDL proficiency and prepare you for the *Advanced VHDL* course.

In this three-day course, you will gain valuable hands-on experience. Incoming students with little or no VHDL knowledge will finish this course empowered with the ability to write efficient hardware designs and perform high-level HDL simulations.

Level – Fundamental to Intermediate

Course Duration – 3 days

Price – 1800\$ or 18 Training Credits

Course Part Number – LANG11000-10-ILT

Who Should Attend? – Engineers who want to use VHDL effectively for modeling, design, and synthesis of digital designs

Prerequisites

- Basic digital design knowledge

Software Tools

- Xilinx ISE® Foundation™ software 10.1 with the ISE Simulator

After completing this comprehensive training, you will have the necessary skills to:

- Write RTL VHDL code for synthesis
- Write VHDL testbenches for simulation
- Create Finite State Machines (FSMs) by using VHDL
- Target and optimize Xilinx FPGAs by using VHDL
- Create RAM and ROM data structures
- Use VHDL scalar and composite data types
- Run a simulation by using VITAL libraries
- Use the VHDL textio package during simulation
- Create and manage designs within the ISE software design environment

Course Outline

Day 1

- Course Agenda
- Hardware Modeling Overview
- VHDL Language Concepts
- **Lab 1:** Building Hierarchy
- Introduction to Testbenches
- **Lab 2:** VHDL Simulation and RTL Verification
- Signals and Data Types
- VHDL Operators and Expressions
- **Lab 3:** Memory

Day 2

- Concurrent and Sequential Statements
- **Lab 4:** Clock Divider and Address Counter
- Controlled Operation Statements
- **Lab 5:** n-bit Binary Counter and RTL Verification
- VITAL: VHDL Initiative toward ASIC Libraries
- **Lab 6:** Timing Simulation
- Behavioral to RTL Coding

Day 3

- Finite State Machines
- **Lab 7:** Finite State Machines
- Targeting Xilinx FPGAs
- **Lab 8:** Implement and Download
- Functions and Procedures
- Advanced Process Statements
- **Lab 9:** Text I/O

Lab Description

The labs for this course provide a practical foundation for creating synthesizable RTL code. All aspects of the design flow are covered in the labs. You will write, synthesize, simulate, and implement all the labs. The focus of the labs is to write code that will optimally infer reliable and high-performance circuits. The labs culminate in a functional calculator that you will verify in simulation.

Register Today

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