After completing this comprehensive training, you will have the necessary skills to:

- Describe how the FPGA architecture lends itself to parallel computing
- Explain how the Vitis unified software environment helps software developers focus on applications
- Describe the Vitis (OpenCL API) execution model
- Analyze the OpenCL API memory model
- Create kernels from C, C++, or RTL IP using the RTL Kernel Wizard
- Apply host code optimization and kernel optimization techniques
- Move data efficiently between kernel and global memory
- Profile the design using the Vitis analyzer tool

Course Specification

Course Outline

Day 1

Vitis Tool Flow

- Introduction to the Vitis Unified Software Platform
  Explains how software/hardware engineers and application developers can benefit from the Vitis unified software environment and OpenCL framework. (Lecture)
- Vitis IDE Tool Overview
  Describes the elements of the development flow, such as software emulation, hardware emulation, and system run as well as debugging support for the host code and kernel code. (Lecture, Lab)
- Vitis Command Line Flow
  Introduces the Vitis environment makefile flow where the user manages the compilation of host code and kernels. (Lecture, Lab)

Basics of Hardware Acceleration

- Introduction to Hardware Acceleration
  Outlines the fundamental aspects of FPGAs, SoCs, and ACAPs that are required to guide the Vitis tool to the best computational architecture for any algorithm. (Lecture)

Alveo Data Center Accelerator Cards

- Alveo Data Center Accelerator Cards Overview
  Describes the Alveo Data Center accelerator cards and lists the advantages of these cards and the available software solutions stack. (Lecture)
- Alveo Accelerator Card Ecosystem Partner Solutions Overview
  Outlines the partner solutions available in the cloud and on premises for Alveo Data Center accelerator cards. (Lecture)

Getting Started with Alveo Data Center Accelerator Cards

- Getting Started with Alveo Data Center Accelerator Cards
  Describes the hardware and software installation procedures for the Alveo Data Center accelerator cards. (Lecture)

Introduction to the Nimbix Cloud

- Introduction to the Nimbix Cloud
  Describes the Nimbix Cloud, the availability of the Alveo Data Center accelerator cards in the Nimbix Cloud, and how to run a design on the Nimbix Cloud. (Lecture)

Vitis Execution Model and XRT

- Vitis Execution Model and XRT
  Describes the XRT and the OpenCL APIs used for such as setting up the platform, executing the target device and post-processing. (Lecture, Lab)
- Synchronization
  Describes OpenCL synchronization techniques such as events, barriers, blocking write/read, and the benefit of using out-of-order execution. (Lecture, Lab)

Day 2

NDRange (Optional)

- Introduction to NDRanges
  Explains the basics of NDRange (N dimensional range) and the OpenCL execution model that defines how kernels execute with the NDRange definition. (Lecture)
- Working with NDRanges
  Outlines the host code and kernel code changes with respect to NDRange. Also explains how NDRange works and the best way to represent the work-group size for the FPGA architecture. (Lecture)
Design Analysis
- Profiling
  Describes the different reports generated by the tool and how to view the reports that help to optimize data transfer and kernel optimization using the Vitis analyzer tool. {Lecture}
- Debugging
  Explains the support for debugging host code and kernel code as well as tips to debug the system. {Lecture}

Kernel Development
- Introduction to C/C++ based Kernels
  Describes the trade-offs between C/C++, OpenCL, and RTL applications and the benefits of C-based kernels. {Lecture, Lab}
- Using the RTL Kernel Wizard to Reuse Existing IP as Accelerators
  Describes how the Vitis unified software development provides RTL kernel developers with a framework to integrate their hardware functions into an application running on a host PC connected to an FPGA via a PCIe® interface. {Lecture, Lab}

Optimization Methodology Guide
- Optimization Methodology
  Describes the recommended flow for optimizing an application in the Vitis unified software development environment. {Lecture}
- C/C++ based Kernel Optimization
  Reviews different techniques such as loop unrolling, pipelining, and DATAFLOW. {Lecture}
- Host Code Optimization
  Describes the various optimization techniques such as reducing the overhead of kernel enqueuing, and optimizing the data transfer between kernels and global memory. {Lecture}
- Optimizing the Performance of the Design
  Describes the various optimization techniques such as optimizing the host code, data transfer between kernels and global memory and the kernel performance. {Lab}

Libraries
- Vitis Accelerated Libraries
  Reviews available libraries such as BLAS, Fintech, and OpenCV. The xfOpenCV library is a set of 60+ kernels, optimized for Xilinx FPGAs and SoCs, based on the OpenCV computer vision library. {Lecture}

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