Course Outline

Day 1
- Introduction to System Generator
- Simulink Software Basics
- Lab 1: Using the Simulink Software
- Basic Xilinx Design Capture
- Demo: System Generator Gateway Blocks

Day 2
- Lab 2: Getting Started with Xilinx System Generator
- Signal Routing
- Lab 3: Signal Routing
- Implementing System Control
- Lab 4: Implementing System Control

Lab Descriptions
- Lab 1: Using the Simulink Software – Learn how to use the toolbox blocks in the Simulink software and design a system. Understand the effect sampling rate.
- Lab 2: Getting Started with Xilinx System Generator – Illustrates a DSP48-based design. Perform hardware co-simulation verification targeting a Xilinx evaluation board.
- Lab 3: Signal Routing – Design padding and unpadding logic by using signal routing blocks.
- Lab 4: Implementing System Control – Design an address generator circuit by using blocks and Mcode.
- Lab 5: Designing a MAC-Based FIR – Using a bottom-up approach, design a MAC-based bandpass FIR filter and verify through hardware co-simulation by using a Xilinx evaluation board.
- Lab 6: Designing a FIR Filter Using the FIR Compiler Block – Design an embedded FIR filter by using the FIR Compiler block to demonstrate increased productivity. Verify the design through hardware co-simulation by using a Xilinx evaluation board.
- Lab 7: System Generator and Vivado IDE Integration – Embed System Generator models into the Vivado IDE.
- Lab 8: System Generator and Vivado HLS Tool Integration – Generate IP from a C-based design to use with System Generator.
- Lab 9: AXI4-Lite Interface Synthesis – Package a System Generator for DSP design with an AXI4-Lite interface and integrate this packaged IP into a Zynq SoC processor system.
- Lab 10: Model Composer and Vivado IDE Integration - Embed a Model Composer model into the Vivado IDE.
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