After completing this comprehensive training, you will have the necessary customizations.

This course focuses on the UltraScale and 7 series architectures. Check Online Training to view these videos.

Go to www.xilinx.com/training and click the FPGA Design link under Hardware or Software Tools.

- **Vivado® Design Suite**
- **Vivado®-VESS-ILT**
- **Architecture: UltraScale™ and 7 series FPGAs**
- **Demo board (optional): Kintex® UltraScale FPGA KCU105 board or Kintex-7 FPGA KC705 evaluation board**

* Go to www.xilinx.com/training and click the FPGA Design link under Online Training to view these videos.

** This course focuses on the UltraScale and 7 series architectures. Check with Hardent for the specifics of the in-class lab board or other customizations.

### Course Outline

#### Day 1
- UltraFast Design Methodology Summary
- CLB Resources
- Introduction to the Vivado Design Suite
- Vivado Design Flows
- **Lab 1**: Vivado Tool Overview
  - Demo: Visualization for Design Analysis
  - Designing with IP
  - Demo: IP Flow
  - Designing with IPI
  - Basic Timing Constraints and STA
  - Demo: Reading Synthesis and Implementation Reports
- **Lab 2**: Vivado Synthesis, Implementation, and Timing Closure

#### Day 2
- I/O Resources
- Other FPGA Resources
- Clocking Resources
- **Lab 3**: Designing with FPGA Resources
- Timing Reports
- **Lab 4**: Basic XDC and Timing Reports
- Synchronous Design Techniques
- FPGA Configuration
- UltraScale+ Families Overview
- Course Summary
- Appendix: Visualization for Analysis
- Appendix: Designing with IP
- Appendix: Designing with IP – IP Integrator Flow Lab

### Lab Descriptions

**Lab 1**: Vivado Tool Overview – Create a project in the Vivado Design Suite. Add files, simulate, and elaborate the design. Review the available reports, analyze the design with the Schematic and Hierarchy viewers, and run a design rule check (DRC). Finally, assign some of the I/O pins using the IO Planner.

**Lab 2**: Vivado Synthesis, Implementation, and Timing Closure – Synthesize and analyze the design with the Schematic viewer, apply a systematic approach to applying timing constraints and timing closure (i.e., understand the Xilinx baselining recommendation). Run basic static timing analysis using the check timing and report clock utilization reports. Implement the design and analyze some timing-critical paths with the Schematic viewer.

Download the bitstream to the demonstration board.

**Lab 3**: Designing with FPGA Resources – Use the Xilinx Clocking Wizard to configure a clocking subsystem to provide various clock outputs and clock buffers to connect clock signals to global clock networks.

**Lab 4**: Basic XDC and Timing Reports – Use timing constraints to improve design performance. Perform static timing analysis before and after implementation to validate the performance results.
Register Today

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