After completing this comprehensive training, you will have the necessary skills to:

- Use the Xilinx Power Estimator spreadsheet to estimate your design’s power consumption after synthesis or implementation to build a better power estimate
- Use Power Report in the Vivado Design Suite to estimate your design’s power consumption after implementation to build the most accurate power estimate
- Use the power_opt implementation options to automatically reduce your design’s power consumption
- Use optimum HDL coding techniques and design practices to reduce your design’s power consumption
- Take advantage of the dedicated hardware features of your FPGA to reduce power consumption

### Lab Descriptions

- **Lab 1:** Power Estimation with XPE – Estimate the resources required based on the high-level design description. Enter the amount of resources and default activity rates for the design and evaluate the estimated power calculated by XPE.
- **Lab 2:** Power Analysis Using the Vivado IDE – Estimate the design’s power consumption at synthesis and implementation with the Vivado power report. Generate a power report by using vectorless and vector-based mode and export the power report to the Power Estimator.
- **Lab 3:** Dynamic Power Estimation with the Vivado IDE – Run the post-synthesis functional simulation of the design to generate a switching activity interchange format (SAIF) file. Create a power report with vectorless and vector-based activity information to verify the design’s dynamic power consumption.

### Course Outline

- Introduction
- FPGA Power Requirements
- Xilinx Power Estimator Spreadsheet (XPE)
- **Lab 1:** Power Estimation with XPE
- Vivado Power Analysis and Optimization
- **Lab 2:** Power Analysis Using the Vivado IDE
- **Lab 3:** Dynamic Power Estimation with the Vivado IDE
- Power Management Design Techniques
- Power Optimization of I/O Resources
- 7 Series Power Management Features
- UltraScale Architecture Power Management Features
- How to Solve a Power Problem
- Worse-Case Thermal Calculations (optional)
- Spartan-6 FPGA Power Management Features (optional)
- Virtex-6 FPGA Power Management Features (optional)
- Power and Temperature Measurement Features (optional)
- Introduction to Partial Reconfiguration (optional)

### Prerequisites

- Essentials of FPGA Design course or equivalent knowledge of FPGA architecture features; the Xilinx implementation software flow and implementation options; reading timing reports; basic FPGA design techniques; global timing constraints and the Constraints Editor
- Intermediate HDL knowledge (VHDL or Verilog)
- Solid digital design background

### Recommended

- Designing for Performance course
- Basic FPGA Architecture: Memory and Clocking Resources
- Vivado Design or System Edition 2014.3
- Architecture: 7 series and UltraScale FPGAs*
- Demo board: N/A

**This course focuses on the 7 series and UltraScale™ architectures. Check with Hardent for the specifics of any course customizations.

### Register Today

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