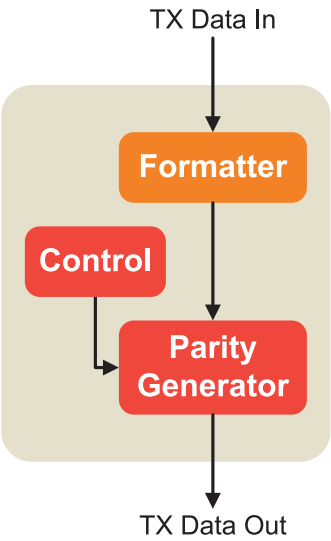
Binary BCH ECC/FEC TX Custom IP Core

Applications

- Satellite communications
- Optical submarine cable systems
- Fault-tolerant SSD storage
- Optical communications

Hardent BCH ECC/FEC TX Custom IP



Hardent's IP portfolio offers customers ready-made solutions to accelerate product development and meet demanding time-to-market schedules.

Developed by a team of experienced FPGA and ASIC designers, Hardent's IP cores have undergone extensive verification and offer proven interoperability and compatibility.

Description

Hardent's binary BCH tool suite is used to produce a high-performance hardware ECC/FEC (Error-Correcting Code/ Forward Error Correction) encoder circuit.

Hardent uses the tool suite, combined with its expertise in ASIC/FPGA and system design, to customize the design of the hardware ECC/FEC encoder IP core to each customer's unique requirements and target application.

The tool suite implements the ECC/FEC function using user-defined parameters.

Key Features

- BCH(n,k)
- User-configurable ECC/FEC parameters
  - Data bus width (w)
  - Codeword length (n), message length (k),
  - Number of parity bits (p)
  - Primitive polynomial and generator polynomial
- Fully synchronous design

Deliverables

- Encrypted RTL source code IP core
- Functional and structural coverage reports
- Comprehensive integration guide
- Technical support and maintenance updates

CUST-BCHFEC-TX _prodbrief-v1.0

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