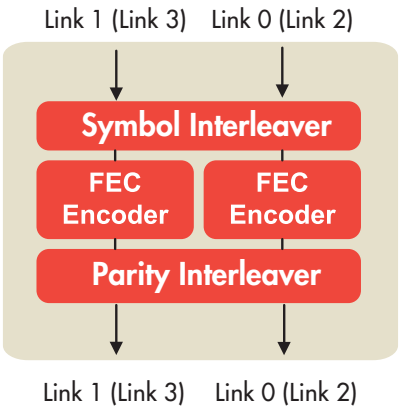
# VESA DisplayPort 2.0 FEC TX IP Core

## Applications

- GPUs
- Desktops & laptops
- UHD TVs and set-top boxes
- USB Type-C & DisplayPort products
- Tablets & mobiles

## Hardent DP 2.0 FEC TX IP

From
PHY Symbol Generator and CDI




To
Precoding and Parallel To Serial Converter

### Description

The DisplayPort™ Forward Error Correction (FEC) Transmitter IP Core implements Reed-Solomon FEC and symbol interleaving as specified by the VESA DisplayPort 2.0 specification. Forward Error Correction is required to ensure low bit error rate at UHBR link rates and glitch-free Display Stream Compression (DSC) bitstream transport.

### Key Features

- VESA DisplayPort 2.0 compliant
- Reed-Solomon RS(198,194) FEC, 8-bit symbols
- Multiple symbols per clock
- Two-way interleaving for 1-, 2- and 4-lane modes (4-lane mode requires 2 FEC IP core instances)

### Deliverables

- Encrypted RTL source code IP core
- Functional and structural coverage reports
- Comprehensive integration guide
- Technical support and maintenance updates

### Product Options

- IP customization and integration services available on request
- Multi-project licenses available
- UVM verification bindable modules

Hardent's IP portfolio offers customers ready-made solutions to accelerate product development and meet demanding time-to-market schedules.

Developed by a team of experienced FPGA and ASIC designers, Hardent's IP cores have undergone extensive verification and offer proven interoperability and compatibility.

VESA MEMBER



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