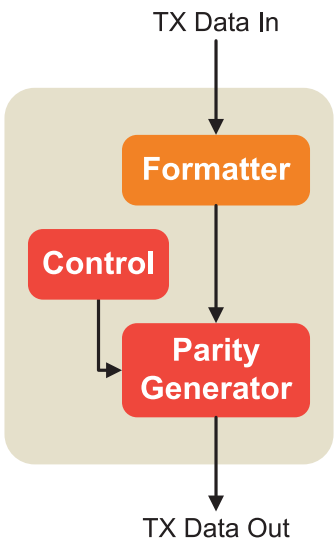
Parallel Reed-Solomon ECC/FEC TX Custom IP Core

Applications

- Optical links
- Ethernet
- High-speed electrical links
- Fault-tolerant SSD storage
- Deep space transmission and telemetry

Hardent PRS ECC/FEC TX Custom IP Core



Hardent's IP portfolio offers customers ready-made solutions to accelerate product development and meet demanding time-to-market schedules.

Developed by a team of experienced FPGA and ASIC designers, Hardent's IP cores have undergone extensive verification and offer proven interoperability and compatibility.

Description

Hardent's ECC/FEC (Error-Correcting Code/Forward Error Correction) proprietary tool suite implements Reed-Solomon algorithms with a high-performance parallel architecture.

Hardent uses the tool suite, combined with its expertise in ASIC/FPGA and system design, to customize the design of the hardware ECC/FEC encoder IP core to each customer's unique requirements and target application.

The tool suite implements the ECC/FEC encoder function using user-defined parameters, including the level of parallelization (symbol per clock) of the circuit, in order to allow for optimization of data throughput and/or gate count.

Key Features

- RS(n,k)
- User-configurable ECC/FEC parameters
  - Bits per symbol (m)
  - Codeword length (n), message length (k)
  - Number of parity symbols (2t)
  - Primitive polynomial and generator polynomial
- Configurable parallelization level (symbols per clock cycle)
- Fully synchronous design

Deliverables

- Encrypted RTL source code IP core
- Functional and structural coverage reports
- Comprehensive integration guide
- Technical support and maintenance updates

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