Learning Path

Our learning path is designed to help you plan your personal development and develop the skills you need to be successful in your career.
Xilinx & Verification Learning Path

Level 1
- VHDL for Design
- Verilog for Design
- SystemVerilog for Design
- Tcl Scripting for Vivado

Level 2
- Vivado Essentials
- US/US+ Architectures
- Zynq US+ RFSoC
- DSP Primer
- Migrating to Vitis IDE
- Embedded SW Design
- Embedded HW Design
- US/US+ Transceivers

Level 3
- Vivado Productivity
- Zynq US+ MPSoC
- Vitis Acceleration
- Vitis in the Cloud
- Vitis on the Edge
- Memory Interfaces
- Signal Integrity
- Adv. Embedded SW Design
- Adv. Embedded HW Design
- Adv. XDC & STA
- Debugging Techniques
- Partial Reconfiguration
- HLS
- Algorithm Optimization
- PetaLinux
- SysGen for DSP

Level 4
- Adv. Timing Closure
- Versal ACAP Architecture
- Advanced HLS
- Vitis AI

NEW
- SystemVerilog for Verification
- UVM
- Adv. UVM

Standard Xilinx Course
- Hardent Exclusive
- Coming Soon by Xilinx
- Coming Soon by Hardent
Want to know more?

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