**Key Features**

- **VESA Display Stream Compression (DSC) 1.2a compliant**
- **Supports all DSC 1.2a mandatory encoding mechanisms**
  - MMAP, BP, MPP, and ICH
- **Input buffering compatible with transport stream over video interfaces**
- **Configurable maximum display resolution**
  - Up to 4K (4096x2160), 5K (UHD+), and 8K (FUHD)
- **8, 10, 12, 14, and 16 bits per video component**
- **YCbCr and RGB video output format**
- **4:4:4, 4:2:2, and 4:2:0 native coding**
- **Resilient to bitstream corruption**
- **3 pixels / clock internal processing architecture in 4:4:4**
- **6 pixels / clock internal processing architecture in 4:2:2 and 4:2:0**
- **Parameterizable number of parallel slice decoder instances (1, 2, or 4) to adapt to the capability of the technology and target display resolutions used**
- **Multiple slices per line in each decoder instance supported (up to 4 slices)**
- **Decode up to 16 slices per line**
- **Optional DSC features can be disabled to improve area**
- **100% verification coverage based on UVM environment**
- **Verified against the VESA DSC 1.2a C model using a comprehensive test image library**
- **Backward compatible with DSC 1.1**

**Deliverables**

- Encrypted RTL source code IP core
- Functional and structural coverage reports
- Comprehensive integration guide
- Technical support and maintenance updates

**Product Options**

- IP customization and integration services available on request
- Multi-project licenses available
- UVM verification bindable modules