Hardent DSC Encoder IP

Key Features

- VESA Display Stream Compression (DSC) 1.1 compliant
- Supports all DSC 1.1 mandatory encoding mechanisms
  - MMAP, BP, MPP, and ICH
- Output buffering compatible with transport stream over video interfaces
- Configurable maximum display resolution
  - Up to 4K (4096x2160), 5K (UHD+), and 8K (FUHD)
- 8 and 10 bits per video component
- YCbCr and RGB 4:4:4 video input format
- 1 pixel / clock internal processing architecture
- Parameterizable number of parallel slice encoder instances (1, 2, or 4) to adapt to the capability of the technology and target display resolutions used
- Multiple slices per line in each encoder instance supported
- 100% verification coverage based on UVM environment
- Verified against the VESA DSC 1.1 C model using a comprehensive test image library

Deliverables

- Encrypted RTL source code IP core
- Functional and structural coverage reports
- Comprehensive integration guide
- Technical support and maintenance updates

Product Options

- IP customization and integration services available on request
- Multi-project licenses available
- UVM verification bindable modules
- FPGA evaluation and prototyping platform

Hardent’s IP portfolio offers customers ready-made solutions to accelerate product development and meet demanding time-to-market schedules.

Developed by a team of experienced FPGA and ASIC designers, Hardent’s IP cores have undergone extensive verification and offer proven interoperability and compatibility.