Hardent DSC 1.2a
For Test Equipment

Description
The Hardent VESA DSC 1.2a Encoder IP Core for test equipment provides an optimized implementation of the VESA Display Stream Compression (DSC) 1.2a standard, using video frame repetition and a frame buffer to minimize the resources required in an FPGA implementation of a UHD video stream.

For example, using the DSC 1.2a IP core would allow the implementation of a UHD 4K60fps interface with only 2 DSC hard slice encoders, instead of 8 hard slice encoders required by the regular configuration. Depending on the approach taken, the input can be either 4K15fps, or 1 frame out of every 4 of a 4K60fps video.

Key Features
- VESA Display Stream Compression (DSC) 1.2a compliant
- 2 slices per line encoding (for 4K panel compatibility)
- Standard compression ratios of 2:1 and 3:1
- Available for Xilinx (with native or AXI interfaces) and Intel (with native or Avalon interfaces) FPGAs

Deliverables
- IP containing DSC encoder netlist
- IP specification
- Testbench
- Vector-based tests of a typical 4K image encoding
- Testbench user guide

Product Options
- IP customization and integration services available on request
- Multi-project licenses available

Hardent’s IP portfolio offers customers ready-made solutions to accelerate product development and meet demanding time-to-market schedules.

Developed by a team of experienced FPGA and ASIC designers, Hardent’s IP cores have undergone extensive verification and offer proven interoperability and compatibility.

Applications
- Display test equipment
- FPGA prototyping

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