Hardent DSC Decoder IP
For Xilinx FPGAs

Key Features

• VESA Display Stream Compression (DSC) 1.2a compliant
• Supports all DSC 1.2a mandatory and optional encoding mechanisms
• Backward compatible to DSC v1.1
• Configurable maximum display resolution up to 8K (FUHD)
• 8, 10, 12 bits per video component
• YCbCr and RGB video output format
• 4:4:4, 4:2:2, and 4:2:0 native coding
• Resilient to bitstream corruption
• 3 pixels / clock internal processing architecture in 4:4:4
• 6 pixels / clock internal processing architecture in 4:2:2 and 4:2:0
• Parameterizable number of parallel slice decoder instances (1, 2, 4, 8) to adapt to the capability of the technology and target display resolutions used
• Automatic run time configuration of the number of parallel slice decoder instances in use
• Support for Xilinx® 7 Series, UltraScale™, and UltraScale+™ FPGAs
• AXI-S interfaces for easy integration in the IP Vivado® integrator
• AXI-Lite interface for register access
• PPS 128 bytes block decoding
• Compliant solution for DisplayPort 1.4™ or HDMI 2.1
• Compatibility for slices per line requirements
• Supports flexible usage models and design architecture (inline decoding or panel frame buffer decoding)

Deliverables

• IP for Xilinx Vivado Design Suite containing DSC Decoder core in netlist format, AXI-S Interface, and AXI-Lite Registers modules in RTL
• IP specification
• Comprehensive integration guide
• Technical support and maintenance updates
• Integration or design services available on request

Hardent’s IP portfolio offers customers ready-made solutions to accelerate product development and meet demanding time-to-market schedules.

Developed by a team of experienced FPGA and ASIC designers, Hardent’s IP cores have undergone extensive verification and offer proven interoperability and compatibility.

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