How to Design a High-Speed Memory Interface

CONN-MIF-ILT (v1.0H)

**Course Description**

This course teaches hardware designers who are new to high-speed memory I/O to design a memory interface in Xilinx FPGAs. It introduces designers to the basic concepts of high-speed memory I/O design, implementation, and debug using Xilinx 7 series FPGAs.

Additionally, students will learn about the tools available for high-speed memory interface design, debug, and implementation of high-speed memory interfaces.

The major memory types covered are DDR2 and DDR3. The following memory types are covered on demand: RLDRAMII, LPDDR2, and QDRII+. Labs are available for DDR3 on the Kintex®-7 FPGA KC705 board.

**Level** – Connectivity 3

**Course Duration** – 2 days

**Price** – $1600 or 16 Training Credits

**Course Part Number** – CONN-MIF-ILT

**Who Should Attend?** – FPGA designers and logic designers

**Prerequisites**

- VHDL or Verilog experience or Designing with VHDL or Designing with Verilog course
- Familiarity with logic design: state machines and synchronous design
- Very helpful to have:
  - Basic knowledge of FPGA architecture
  - Familiarity with Xilinx implementation tools
- Nice to have:
  - Familiarity with I/O basics
  - Familiarity with high-speed I/O standards

**Software Tools**

- Vivado® Design or System Edition 2015.1
- Mentor Graphics Questa Advanced Simulator 10.3d
- Mentor Graphics HyperLynx SI 9.x

**Hardware**

- Architecture: 7 series FPGAs*
- Demo board: Kintex®-7 FPGA KC705 board*

* This course focuses on the 7 series architecture. Check with Hardent for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Identify the FPGA resources required for memory interfaces
- Describe different types of memories
- Utilize Xilinx tools to generate memory interface designs
- Simulate memory interfaces with the Xilinx Vivado simulator
- Implement memory interfaces
- Identify the board design options for the realization of memory interfaces
- Test and debug your memory interface design
- Run basic memory interface signal integrity simulations

**Course Outline**

**Day 1**

- Course Introduction
- 7 Series FPGAs Overview
- Memory Devices Overview
- 7 Series Memory Interface Resources
- Memory Controller Details and Signals
- MIG Design Generation

**Lab Descriptions**

**Day 1**

- **Lab 1:** MIG Core Generation
- **Lab 2:** MIG Design Simulation
- **Lab 3:** MIG Design Implementation

**Day 2**

- **Lab 4:** MIG Design Debugging
- **Lab 5:** MIG in IP Integrator
- **Lab 6:** DDR3 Signal Integrity Simulation (optional)

**Register Today**

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Email: training@hardent.com
Telephone: 514-284-5252

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