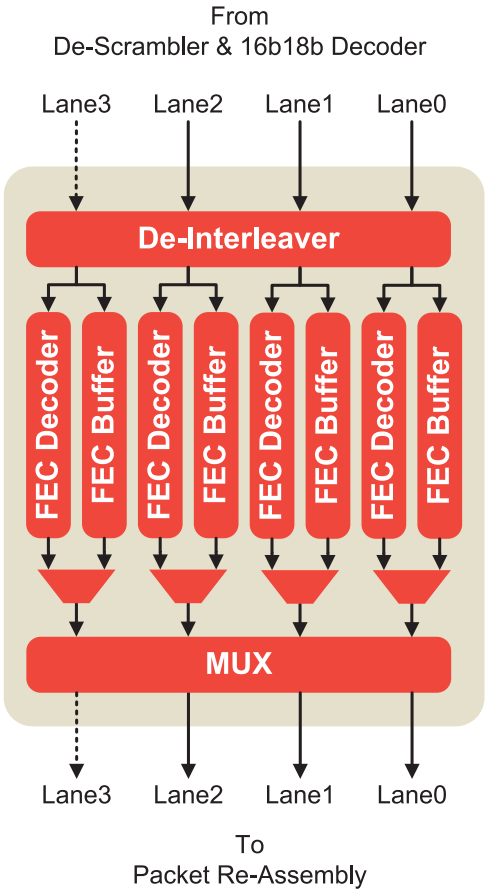
HDMI 2.1 FEC RX IP Core

Applications

- UHD monitors
- UHD TVs & home theaters
- HDMI 2.1 hubs & accessories
- Professional video equipment

Hardent HDMI 2.1 FEC RX IP



Description

The HDMI Forward Error Correction (FEC) Receiver IP Core implements Reed-Solomon FEC and symbol de-interleaving/ de-mapping as specified by the HDMI 2.1 specification.

Forward Error Correction is required to ensure glitch-free operation in Fix Rate Lane (FRL) mode, a packet mode introduced in HDMI 2.1. FRL allows for the use of Display Stream Compression (DSC) bitstream transport.

Key Features

- HDMI 2.1 compliant
- Reed-Solomon RS(255,251) FEC, 8-bit symbols
- Supports 3-lane and 4-lane operation
- Includes error counters

Deliverables

- Encrypted RTL source code IP core
- Functional and structural coverage reports
- Comprehensive integration guide
- Technical support and maintenance updates

Product Options

- IP customization and integration services available on request
- Multi-project licenses available
- UVM verification bindable modules

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