Course Description

This one-day course provides an introduction to the VESA DSC v1.1 video compression standard. The course begins with an introduction to the basics of the underlying structure of DSC video algorithms and evolves to explore DSC applications, usage models, system architecture, and implementation challenges for DSC encoder and decoder designs. The course concludes with an overview of the resources available at VESA, as well as considerations and practical recommendations on how to design a product compatible with the VESA DSC v1.1 video compression standard.

Price – $800 USD
Course Duration – 1 day
Who Should Attend?
• System architects, engineers and designers who have an interest in using DSC for mobiles, tablets, TV and other display applications.

Recommended Prerequisites
• It is highly recommended that you become a VESA member prior to attending this course. The application form for VESA membership can be found on the VESA website.

Recommended Reading
• VESA Display Stream Compression White Paper

Course Outline

DSC Introduction
• Basic concepts and origins of DSC
• System benefits, financial considerations and target market segments
• Visually lossless quality assessment

VESAs DSC Standard
• DSC v1.1 fundamentals: Understanding DSC compression, slices encoding and decoding. Rate control and rate buffer.
• DSC v1.1 algorithms: Prediction modes, prediction loops, indexed color history, encoding decision process, VLC encoding, sub-stream multiplexing and slice multiplexing.
• Overview of DSC v1.2

Applications, Usage Models and System Architecture
• System architecture overview
• Interoperability challenges
• DSC adoption by transport interface standards
• MIPI DSI 1.2 applications: video and command modes
  o Integration with DSI Host Controllers and Peripherals
• Embedded DisplayPort 1.4 applications
  o Single and Multi-Stream outputs
• DSC and error resilience
• Compliance test guide

DSC Encoder and Decoder Implementation Challenges
• Product requirements and performance objectives
• Decoder architecture elements: Data flow and pipelining. Context switch. Algorithm sub-blocks implementation. Input Buffer, sub-stream de-multiplexing, VLC Decoder, Rate Controller and rate buffer sizing.

Designing a System with DSC: How to Get Started?
• VESA information available: C-model and standard specifications
• Other resources available

Register Today

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Email: training@hardent.com
Telephone: 514-284-5252