**Course Description**

This 3-day course teaches designers to write efficient, accurate RTL code for synthesis as well as basic testbenching and verification techniques.

This course is intended for designers who are new to Verilog and who wish to become familiar with the language, with a particular emphasis on writing RTL code for synthesis. We also cover how to construct testbenches for unit level verification of your RTL code.

This course continuously mixes lecture and exercise. There is a simulation exercise for most topics providing a very hands-on experience. Synthesizable constructs are clearly identified and appropriate synthesis coding techniques discussed.

**Level** – VD 1  
**Course Duration** – 3 days  
**Price** – $2400

**Who Should Attend?** Design Engineers who want to learn how to write synthesizable RTL code in Verilog as well as simple testbenches to verify the design at a block level.

**Prerequisites**
- A background in digital design
- Programming experience in C or another language is recommended

**Software Tools**
- Questa Simulator 10.4c

After completing this comprehensive training, you will have the necessary skills to:
- Write Verilog procedural code correctly
- Explain how to declare sequential, combinational, and latch-based structures in Verilog RTL
- Describe the basic steps of the synthesis process
- Write a Verilog testbench to exercise and verify your design code to the block level

**Course Outline**

- Verilog modeling
- Using your Simulator
- Verilog basics
- Procedural assignments
- Design a sequential pipe
- Synthesizing your design
- Operators
- Programming statements
- Sensitivity lists
- Continuous assignments
- Primitives
- Tasks
- Functions
- Timing accuracy
- Verification using Verilog
- Bi-directionals
- Synthesis issues
- Finite State machines (exercise)

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