Course Description
Learn how to construct, implement, and download a Partially Reconfigurable (PR) FPGA design using the Vivado® Design Suite. This course covers both the tool flow and mechanics of successfully creating a PR design.

The emphasis is on:
- Identifying best design practices and understanding the subtleties of the PR design flow
- Using the PR controller and PR decoupler IP in the PR process
- Implementing PR in an embedded system environment
- Applying appropriate debugging techniques on PR designs
- Employing best practice coding styles for a PR system

Course Specification
- Floorplanning
- Timing constraints and analysis
- Implement a PR system using the PRC IP
- Implement a PR system in an embedded environment
- Debug PR designs

Course Outline
Day 1
- Introduction to Partial Reconfiguration
  - Demo: Introduction to Partial Reconfiguration
  - Partial Reconfiguration Flow
  - Lab 1: Partial Reconfiguration Tool Flow
  - Lab 2: Partial Reconfiguration Project Flow
  - Lab 3: Floorplanning the PR Design
  - Lab 4: Partial Reconfiguration: Managing Timing
  - Demo: Partial Reconfiguration Controller (PRC) IP

Day 2
- Partial Reconfiguration: Managing Timing
  - Lab 5: Partial Reconfiguration Timing Analysis and Constraints
  - Partial Reconfiguration in Embedded Systems
  - Lab 6: Partial Reconfiguration in Embedded Systems
  - Debugging Partial Reconfiguration Designs
  - Lab 7: Debugging a Partial Reconfiguration Design
  - Partial Reconfiguration Design Recommendations
  - PCIe Core and Partial Reconfiguration

Lab Descriptions
- Lab 1: Partial Reconfiguration Tool Flow – Illustrates the basic Vivado Design Suite Partial Reconfiguration flow. At the completion of this lab, you will download a partial bitstream to the demo board via the JTAG connection.
- Lab 2: Partial Reconfiguration Project Flow – Illustrates Partial Reconfiguration (PR) project flow in the Vivado® Design Suite. At the end of this lab, you will be able to create multiple RMs and configurations using Partial Reconfiguration Wizard.
- Lab 3: Floorplanning the PR Design – Illustrates how to create efficient PBlocks for a Partial Reconfiguration design. At the end of this lab, you will understand the impact of the SNAPPING_MODE property for a Pblock.
- Lab 4: Using the Partial Reconfiguration Controller in a PR Design – Illustrates using the PRC IP and hardware triggers to manage partial bitstreams.
- Lab 7: Debugging a Partial Reconfiguration Design – Demonstrates using ILA cores to debug PR designs and shows which signals to monitor during debugging.
Register Today

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